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EECE488: Analog CMOS Integrated Circuit Design

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Low Voltage CMOS SAR ADC Page 8 Functional Decomposition This section breaks the design down into 3 separate levels. Level 0 depicts a basic block diagram showing all of the inputs and outputs of the ADC. Level 1 depicts the basic flow of the signals in the design and how the signal processing works.

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CMOS Analog Integrated Circuit Design

BASIC LINEAR DESIGN 1.8 Doing a little simple arithmetic we then can come to the conclusion of eq. 1.1: Figure 1.6: Noninverting Amplifier gain Now we examine the noninverting case in more detail. Referring to Figure 1.6, the input voltage is applied to the noninverting terminal. The output voltage drives a voltage divider consisting of R_{fb} and R_{in} .

CHAPTER 1: THE OP AMP - analog.com

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INTRODUCTION TO RF CMOS IC DESIGN FOR WIRELESS

processing analog signals. A longer settling time implies that the rate of processing analog signals must be reduced. In the following design, a 10mV signal must be resolved using the comparator in Figure 2 and 3. The power supply rails are $V_{DD}=5V$ and $V_{SS}=-5V$. That is, the output will swing by 10V (from $-5V$ to

CMOS COMPARATOR 1. Comparator Design Specifications

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CMOS Schmitt trigger and its transfer characteristic I_o (a) (C) Fig. 2. N-subcircuit driven by a voltage source: (a) circuit; (b) current-voltage characteristic; (c) superposition of N- and P-subcircuit characteristics. When the voltage V_i is very small, transistor M_3 will be off, and M_1 and M_2 are in the triode mode of operation.

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